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New Crystallization Method of Amorphous Silicon by Selective Area Heating for Stamp Process

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We propose a new crystallization technique called selective area heating. In this study, we investigated a new technique for high-reliability selective area crystallization of a-Si films that does not cause thermal damage to glass substrates. We reduced the crystallization time as compared to the conventional solid phase crystallization method using a stamp-type isolated thin heater. The thin heater was fabricated with a layer of Pt on a quartz substrate via Ta adhesion and capping layers. A crystalline transverse optic phonon peak at about 519 cm^{-1} was seen in Raman scattering spectra, showing that the films were crystallized. The poly-Si grain size was found to be smaller than 100 nm, and the dendritic structure was found using scanning electron microscopy.

Keywords: crystallization; poly crystalline; selective area heating; solid phase crystallization; stamp process; thermal budget

PACs Numbers: Codes 64.70 kg and 65.60.+a

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INTRODUCTION

One of the most important materials for fabricating active matrix organic light emitting diode (AMOLDE) and solar cell is polycrystalline silicon (poly-Si). Poly-Si provides higher device reliability, better electrical performance, and a lower defect density than amorphous silicon (a-Si). Conventional poly-Si materials can be prepared using various techniques to crystallize a-Si, including solid-phase crystallization (SPC) [1], rapid thermal annealing (RTA) [2], metal induced crystallization (MIC) [3], and excimer laser annealing (ELA) [4]. However, SPC using low temperature annealing ($\sim$600°C) requires a long annealing time and a high thermal budget. RTA has been proposed to reduce crystallization time, however it requires a high thermal budget which causes problems such as glass bending. MIC has been employed to reduce crystallization time and temperature by making use of the catalytic effect of metals such as Ni [5], Pd [6], and Al [7], but these metals introduce a contamination in the active layer. ELA is one of the most promising crystallization technologies for obtaining high-quality poly-Si films using a low temperature process. The disadvantages of ELA are its cost and uniformity problems for the backplane TFTs for AMOLED. Thus, these technologies requiring a high temperature, long annealing times, and high cost are not suitable for a large and flexible display.

In this paper, we suggest a new crystallization technique for high-reliability selective area crystallization of a-Si films using selective area heating (SAH) that would not induce thermal damage on the glass substrates. We reduced the crystallization time as compared to the conventional SPC method using a stamp-type isolated thin heater. We propose this stamp process for mass production and large area displays.

EXPERIMENTAL DETAILS

A 2000 Å-thick SiN_x film was deposited on a glass substrate by plasma enhanced chemical vapor deposition (PECVD). Then, 2000 Å-thick a-Si films were deposited by PECVD using SiH_4 as a source gas. The substrate temperature was kept at 150°C during deposition. Figure 1(a) shows the experimental setup for the SAH which was provided by a stamp-type thin heater. The heater's height was controlled by micro-controller. The distance between the heater and sample was about 0.3 mm. The 1 cm $\times$ 1 cm sample was loaded on a plate in the vacuum chamber where the SAH was performed using an applied

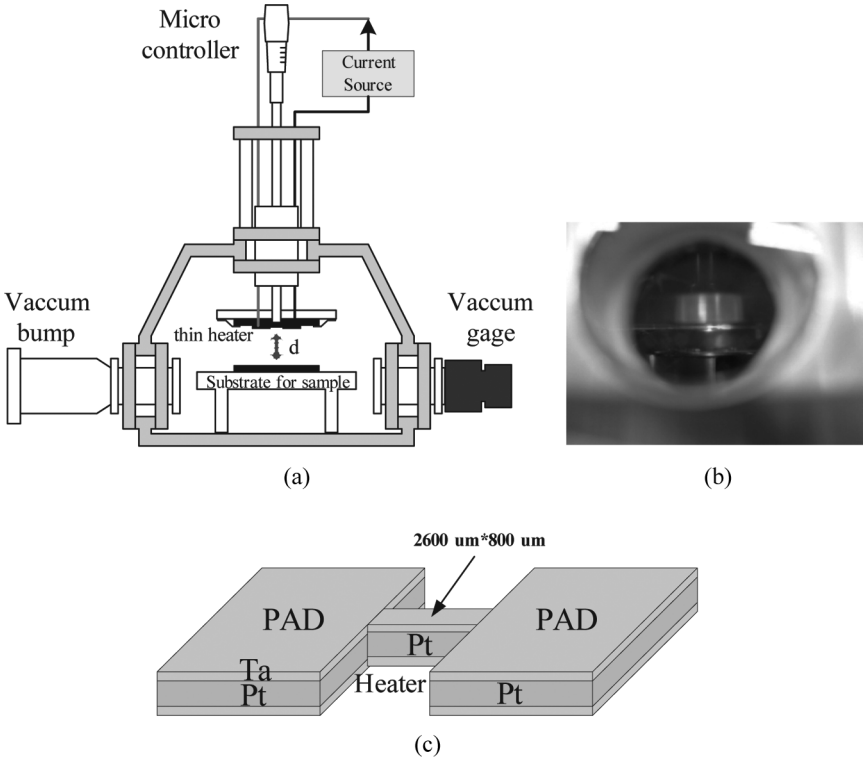

FIGURE 1 (a) Experimental setup; (b) emission image of thin heater; and (c) structure of thin heater.

current in the heater. The thin heater was heated by the joule heating method. Figure 1(b) shows an emission image of the heater at 1.8 A. The surface temperature of the heater was measured by an optical pyrometer. In order to selectively heat the a-Si film, a Pt thin heater was patterned on a quartz substrate with two pads as shown in Figure 1(c). A 5000 Å-thick Pt film was deposited by DC sputtering. Pt was a suitable material for the thin heater because of its high melting point (1,769°C), high resistance to oxidation, and ease of deposition [8].

The heater was degraded by electromigration under high current densities. Thus, the Pt thin heater had two additional layers for improved the reliability: a Ta adhesion layer and a Ta capping layer [8]. These layers reduced the electromigration and increased the lifetime of the Pt thin heater. After crystallization of a-Si films by thin

heater annealing, the properties of the poly-Si were investigated by Raman spectroscopy. Scanning electron microscopy (SEM) was also used to determine the structure of the poly-crystalline after a Secco etching. The diameter of the crystallized Si area after various annealing times was measured by optical microscopy.

RESULTS AND DISCUSSION

Power consumption values were calculated by applying currents and measured voltages. The area of the thin heater was 2,600 μm × 800 μm, μm, and its thickness was 500 nm with a 20 nm Ta adhesion layer and a 50 nm Ta capping layer. The input currents ranged from 1 A to 1.9 A. The power consumption can be described using

$$P = V \times I = I^2 \times R = I^2 \times \rho \frac{L}{Wt} \quad (1)$$

where P is the power consumption, I is the applied current, R is the resistance of the thin heater, W is its width, t is its thickness, L is its length, and ρ is its resistivity. The power consumption per unit area is

$$\frac{P}{A} = I^2 \times \rho \frac{1}{W^2 t} \quad (2)$$

where A is the unit area. We controlled the power consumption and the temperature of the heater by applying current according to this equation. As the applied current increased, the power consumption and temperature of the heater increased as shown in Figure 2.

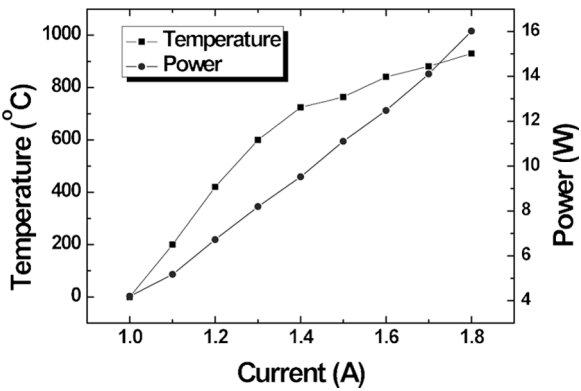

FIGURE 2 Relationship between applied current and surface temperature in thin heater.

The temperature of the Pt thin heater increased linearly up to about 800°C. Above 800°C, the temperature exponentially increased by material degradation like an agglomeration [8]. The electrical resistance could be expressed as

$$R = R_0 \times [1 + \alpha(T - T_0)] \tag{3}$$

where R is the resistance at temperature T, R_0 is the resistance at a reference temperature T_0, and α is the temperature coefficient of resistance equal to $2.86 \times 10^{-3}/°C$ [9]. A temperature range of 200°–1,000°C was achieved. The resistance in the Pt layer was decreased when the applied current and temperature was increased. However, the surface temperature was an indication of the SAH conditions.

Figure 3(a) shows the optical microscopy image of the Si area crystallized using SAH. The crystallized area was more transparent

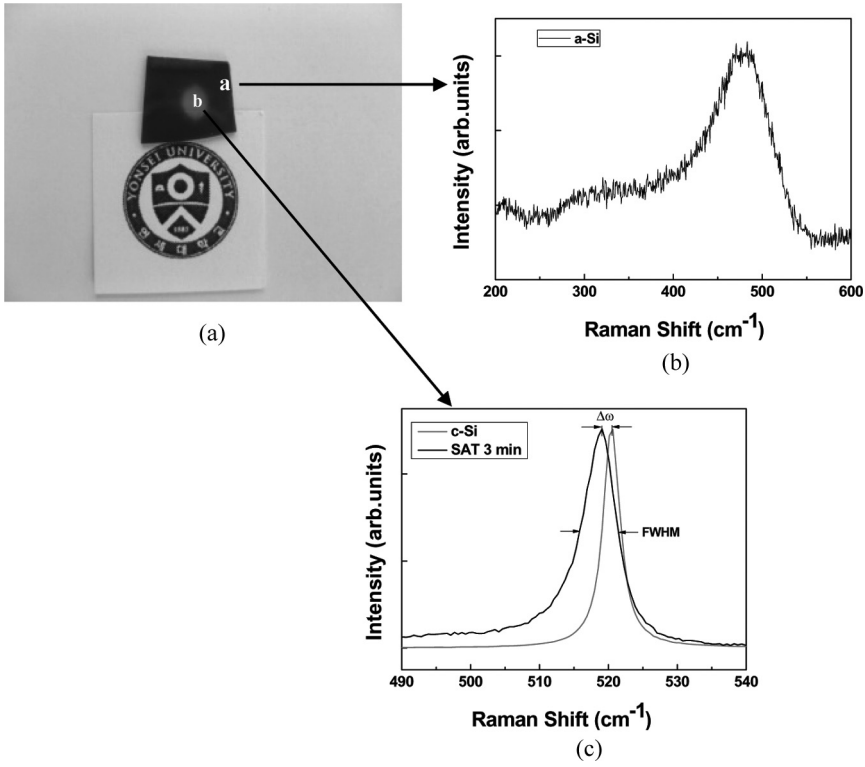

FIGURE 3 (a) The optical microscopy image of the Si area crystallized using SAH; (b) Raman spectra of a-Si; and (c) poly-Si using SAH.

than the a-Si area and showed a circle caused by radiant thermal energy. SAH was induced such that the annealing time was 3 minutes at 1.8 A. The crystallinity of the a-Si films was measured by Raman spectroscopy. The Raman transverse optic (TO) phonon peak of the a-Si films is shown in Figures 3(b) and 3(c). Crystalline TO phonon peaks around 480 cm^{-1} and 519 cm^{-1} were observed at positions "a" and "b". The spectrum at position "a" in Figure 3(a) shows an a-Si crystalline peak. Position "b" is similar to that of a poly-Si peak in material created using SAH. The residual stress in the thin films has been characterized by Raman spectroscopy. There was a report that stress causes a frequency shift, $\Delta\omega$, of the optical-phonon line at $\sim$520 cm^{-1} [10]. The shift in the peak position, about 519 cm^{-1}, indicated the existence of tensile stress [11–13]. The full-width at half-maximum (FWHM) of the optical-phonon line obtained for single crystalline was 3.0 cm^{-1}, and was 6.0 cm^{-1} for SAH poly-Si as shown in Figure 3(c). Finally, the glass substrate showed no damage even though the temperature of the thin heater was above 900°C because the exposed area to the radiant thermal heating depends on the size of the thin film heater which is small.

Figure 4 shows a SEM image of the Secco etched SAH poly-Si films annealed for 3 min by the stamp-type thin heater at an applied current of 1.8 A. We confirmed the structure of SAH poly-Si to be similar to the conventional SPC of a-Si. The grain structure was a dendritic structure with twins extending along the principal axis of the grains [14,15]. The grain sizes were smaller than 100 nm.

As annealing times were increased, the size of the crystallized Si areas increased, as shown in Figure 5. The relationship between

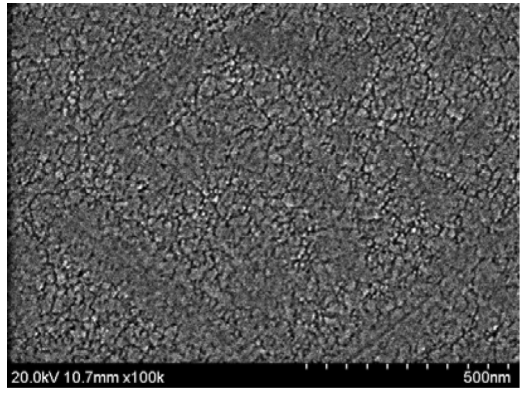

FIGURE 4 SEM image of crystallized Si using SAH.

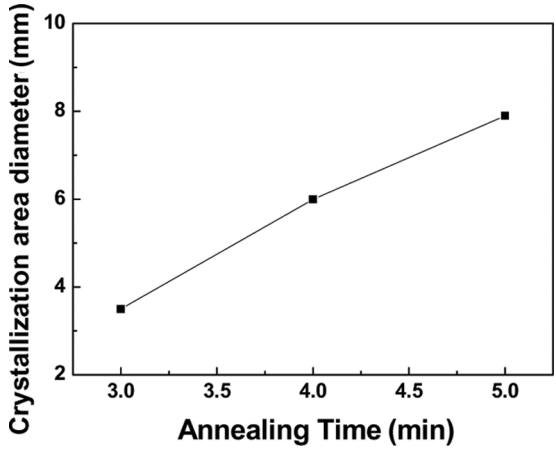

FIGURE 5 Relationship between annealing times and crystallized Si areas.

annealing time and crystallized Si area is as follows:

$$V = \frac{L}{t}\ \mu m/sec \tag{4}$$

where V is the growth velocity of the crystallized Si area, t is the annealing time, and L is the crystallized area diameter. As a result of this equation, the growth velocity of the crystallized Si area was above 35 μm/sec at 1.8 A.

Figure 6 shows the proposed stamp process using a new crystallization technique. With this technology it is possible to crystallize effectively and repeatedly in the active area only. SAH is considered to be a promising technology for the creation of large area display panels using a low cost process.

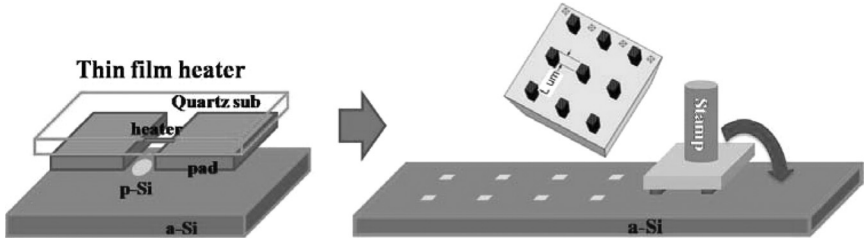

FIGURE 6 Proposed stamp process using a new crystallization technique.

CONCLUSION

We proposed a new crystallization technique for the high-reliability selective area crystallization of a-Si films without any thermal damage on glass substrates. We reduced the crystallization time compared to the conventional SPC method using a stamp-type isolated thin heater. The crystalline TO phonon peak at about 519 cm^{-1} was observed. The poly-Si grain size was found to be smaller than 100 nm with dendritic structures. The proposed stamp process using SAH is suitable for creating large area displays at low cost because it is possible to effectively and repeatedly crystallize a predetermined active area only.

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